

5 Inventor: Clinton O. Fruitman

10

15

20

25

30

35

40

45

50

55

60

65

70

75

80

85

90

95

100

105

110

115

120

125

130

135

140

145

150

155

160

165

170

175

180

185

190

195

200

205

210

215

220

225

230

235

240

245

250

255

260

265

270

275

280

285

290

295

300

305

310

315

320

325

330

335

340

345

350

355

360

365

370

375

380

385

390

395

400

405

410

415

420

425

430

435

440

445

450

455

460

465

470

475

480

485

490

495

500

505

510

515

520

525

530

535

540

545

550

555

560

565

570

575

580

585

590

595

600

605

610

615

620

625

630

635

640

645

650

655

660

665

670

675

680

685

690

695

700

705

710

715

720

725

730

735

740

745

750

755

760

765

770

775

780

785

790

795

800

805

810

815

820

825

830

835

840

845

850

855

860

865

870

875

880

885

890

895

900

905

910

915

920

925

930

935

940

945

950

955

960

965

970

975

980

985

990

995

1000

1005

1010

1015

1020

1025

1030

1035

1040

1045

1050

1055

1060

1065

1070

1075

1080

1085

1090

1095

1100

1105

1110

1115

1120

1125

1130

1135

1140

1145

1150

1155

1160

1165

1170

1175

1180

1185

1190

1195

1200

1205

1210

1215

1220

1225

1230

1235

1240

1245

1250

1255

1260

1265

1270

1275

1280

1285

1290

1295

1300

1305

1310

1315

1320

1325

1330

1335

1340

1345

1350

1355

1360

1365

1370

1375

1380

1385

1390

1395

1400

1405

1410

1415

1420

1425

1430

1435

1440

1445

1450

1455

1460

1465

1470

1475

1480

1485

1490

1495

1500

1505

1510

1515

1520

1525

1530

1535

1540

1545

1550

1555

1560

1565

1570

1575

1580

1585

1590

1595

1600

1605

1610

1615

1620

1625

1630

1635

1640

1645

1650

1655

1660

1665

1670

1675

1680

1685

1690

1695

1700

1705

1710

1715

1720

1725

1730

1735

1740

1745

1750

1755

1760

1765

1770

1775

1780

1785

1790

1795

1800

1805

1810

1815

1820

1825

1830

1835

1840

1845

1850

1855

1860

1865

1870

1875

1880

1885

1890

1895

1900

1905

1910

1915

1920

1925

1930

1935

1940

1945

1950

1955

1960

1965

1970

1975

1980

1985

1990

1995

2000

2005

2010

2015

2020

2025

2030

2035

2040

2045

2050

2055

2060

2065

2070

2075

2080

2085

2090

2095

2100

2105

2110

2115

2120

2125

2130

2135

2140

2145

2150

2155

2160

2165

2170

2175

2180

2185

2190

2195

2200

2205

2210

2215

2220

2225

2230

2235

2240

2245

2250

2255

2260

2265

2270

2275

2280

2285

2290

2295

2300

2305

2310

2315

2320

2325

2330

2335

2340

2345

2350

2355

2360

2365

2370

2375

2380

2385

2390

2395

2400

2405

2410

2415

2420

2425

2430

2435

2440

2445

2450

2455

2460

2465

2470

2475

2480

2485

2490

2495

2500

2505

2510

2515

2520

2525

2530

2535

2540

2545

2550

2555

2560

2565

2570

2575

2580

2585

2590

2595

2600

2605

2610

2615

2620

2625

2630

2635

2640

2645

2650

2655

2660

2665

2670

2675

2680

2685

2690

2695

2700

2705

2710

2715

2720

2725

2730

2735

2740

2745

2750

2755

2760

2765

2770

2775

2780

2785

2790

2795

2800

2805

2810

2815

2820

2825

2830

2835

2840

2845

2850

2855

2860

2865

2870

2875

2880

2885

2890

2895

2900

2905

2910

2915

2920

2925

2930

2935

2940

2945

2950

2955

2960

2965

2970

2975

2980

2985

2990

2995

3000

3005

3010

3015

3020

3025

3030

3035

3040

3045

3050

3055

3060

3065

3070

3075

3080

3085

3090

3095

3100

3105

3110

3115

3120

3125

3130

3135

3140

3145

3150

3155

3160

3165

3170

3175

3180

3185

3190

3195

3200

3205

3210

3215

3220

3225

3230

3235

3240

3245

3250

3255

3260

3265

3270

3275

3280

3285

3290

3295

3300

3305

3310

3315

3320

3325

3330

3335

3340

3345

3350

3355

3360

3365

3370

3375

3380

3385

3390

3395

3400

3405

3410

3415

3420

3425

3430

3435

3440

3445

3450

3455

3460

3465

3470

3475

3480

3485

3490

3495

3500

3505

3510

3515

3520

3525

3530

3535

3540

3545

3550

3555

3560

3565

3570

3575

3580

3585

3590

3595

3600

3605

3610

3615

3620

3625

3630

3635

3640

3645

3650

3655

3660

3665

3670

3675

3680

3685

3690

3695

3700

3705

3710

3715

3720

3725

3730

3735

3740

3745

3750

3755

3760

3765

3770

3775

3780

3785

3790

3795

3800

3805

3810

3815

3820

3825

3830

3835

3840

3845

3850

3855

3860

3865

3870

3875

3880

3885

3890

3895

3900

3905

3910

3915

3920

3925

3930

3935

3940

3945

3950

3955

3960

3965

3970

3975

3980

3985

3990

3995

4000

4005

4010

4015

4020

4025

4030

4035

4040

4045

4050

4055

4060

4065

4070

4075

4080

4085

4090

4095

4100

4105

4110

4115

4120

4125

4130

4135

4140

4145

4150

4155

4160

4165

4170

4175

4180

4185

4190

4195

4200

4205

4210

4215

4220

4225

4230

4235

4240

4245

4250

4255

4260

4265

4270

4275

4280

4285

4290

4295

4300

4305

4310

4315

4320

4325

4330

4335

4340

4345

4350

4355

4360

4365

4370

4375

4380

4385

4390

4395

4400

4405

4410

4415

4420

4425

4430

4435

4440

4445

4450

4455

4460

4465

4470

4475

4480

4485

4490

4495

4500

4505

4510

4515

4520

4525

4530

4535

4540

4545

4550

4555

4560

4565

4570

4575

4580

4585

4590

4595

4600

4605

4610

4615

4620

4625

4630

4635

4640

4645

4650

4655

4660

4665

4670

4675

4680

4685

4690

4695

4700

4705

4710

4715

4720

4725

4730

4735

4740

4745

4750

4755

4760

4765

4770

4775

4780

4785

4790

4795

4800

4805

4810

4815

4820

4825

4830

4835

4840

4845

4850

4855

4860

4865

4870

4875

4880

4885

4890

4895

4900

4905

4910

4915

4920

4925

4930

4935

4940

4945

4950

4955

4960

4965

4970

4975

4980

4985

4990

4995

5000

5005

5010

5015

5020

5025

5030

5035

5040

5045

5050

5055

5060

5065

5070

5075

5080

5085

5090

5095

5100

5105

5110

5115

5120

5125

5130

5135

5140

5145

5150

5155

5160

5165

5170

5175

5180

5185

5190

5195

5200

5205

5210

5215

5220

5225

5230

5235

5240

5245

5250

5255

5260

5265

5270

5275

5280

5285

5290

5295

5300

5305

5310

5315

5320

5325

5330

5335

5340

5345

5350

5355

5360

5365

5370

5375

5380

5385

5390

5395

5400

5405

5410

5415

5420

5425

5430

5435

5440

5445

5450

5455

5460

5465

5470

5475

5480

5485

5490

5495

5500

5505

5510

5515

5520

5525

5530

5535

5540

5545

5550

5555

5560

5565

5570

5575

5580

5585

5590

5595

5600

5605

5610

5615

5620

5625

5630

5635

5640

5645

5650

5655

5660

5665

5670

5675

5680

5685

5690

5695

5700

5705

5710

5715

5720

5725

5730

5735

5740

5745

5750

5755

5760

5765

5770

5775

5780

5785

5790

5795

5800

5805

5810

5815

5820

5825

5830

5835

5840

5845

5850

5855

5860

5865

5870

5875

5880

5885

5890

5895

5900

5905

5910

5915

5920

5925

5930

5935

5940

5945

5950

5955

5960

5965

5970

5975

5980

5985

5990

5995

6000

6005

6010

6015

6020

6025

6030

6035

6040

6045

6050

6055

6060

6065

6070

6075

6080

6085

6090

6095

6100

6105

6110

6115

6120

6125

6130

6135

6140

6145

6150

6155

6160

6165

6170

6175

6180

6185

6190

6195

6200

6205

6210

6215

6220

6225

6230

6235

6240

6245

6250

6255

6260

6265

6270

6275

6280

6285

6290

6295

6300

6305

6310

6315

6320

6325

6330

6335

6340

6345

6350

6355

6360

6365

6370

6375

6380

6385

6390

6395

6400

6405

6410

6415

6420

6425

6430

Presently known polishing techniques are unsatisfactory in several regards. For example, as the size of microelectronic structures used in integrated circuits decreases, and further as the number of microelectronic structures on current and future generation integrated circuits increases, the degree of planarity required increases dramatically. For example, the high degree of accuracy of current lithographic techniques or smaller devices requires increasingly flatter surfaces. Presently known polishing techniques are believed to be inadequate to produce the degree of planarity and uniformity across the relatively large surfaces of silicon wafers used in integrated circuits, particularly for future generations.

Presently known polishing techniques are also unsatisfactory in that the cellular structure of the polishing pad tends to generate heat at the interface between the pad and the workpiece. The presence of heat is problematic in that it tends to dry the slurry in the vicinity of large workpiece centers. As a polishing pad moves radially inward across the surface of a circular wafer, it has been observed that the slurry can dehydrate unevenly across the surface of the workpiece. Consequently, the polishing effect of the pad can be non-uniform across the surface of the workpiece, resulting in non-uniform planarization effects.

Chemical mechanical planarization techniques and materials are thus needed which will permit a higher degree of planarization and uniformity of that planarization over the entire surface of integrated circuit structures.

### Summary of the Invention

In accordance with a preferred exemplary embodiment of the present invention, a chemical mechanical planarization process employs a non-cellular surface or pad in lieu of the traditional cellular polishing pad employed in presently known CMP processes. Such a flat or non-cellular pad dramatically reduces the number of stress concentration points over a given surface area of contact between the polishing pad and the workpiece being polished, resulting in a more uniform planarization across the workpiece surface. In accordance with a further aspect of the present invention, the use of a non-cellular pad also may have the effect of reducing the extent to which the pad bends over device topographies due to the lack of a cellular nap. In accordance with a further aspect of the present invention, to the extent the reduction in asperity density (number of stress concentration points per surface area at the polishing pad) reduces the material removal rate in the polishing process, the pressure between the polishing pad and workpiece may be increased to thereby compensate for the reduction

removal rate. Inasmuch as the increased pressure will be spread out over a greater surface area of contact between the pad and the workpiece, damage to delicate microstructures may be concomitantly minimized.

5 In accordance with a further aspect of the present invention, the use of a non-cellular or substantially flat polishing pad effectively performs a lapping function on the workpiece, to the extent contact forces are distributed over a greater area for a given applied pressure, achieving maximum flatness and planarity on the workpieces being polished.

10 In accordance with a further aspect of the present invention, use of a non-cellular and/or substantially flat pad in lieu of the traditional cellular polishing pads facilitates more uniform slurry distribution, reducing non-uniform effects of planarization on the finished workpieces.

#### Brief Description of the Drawing Figures

The subject invention will hereinafter be described in conjunction with the appended drawing figures, wherein like numerals designate like elements, and:

Figure 1 is a schematic diagram of an exemplary foam polishing pad operating on an exemplary silicon workpiece in an abrasive slurry environment;

Figure 2 is a concept diagram illustrating chemical aspects of a traditional chemical mechanical planarization process;

Figure 3 is a close-up view of an exemplary known polishing pad, showing stress concentration points;

Figure 4(a) is a schematic cross-section view of an exemplary section of an integrated circuit, showing microelectronic structures imbedded in a dielectric layer, shown in conjunction with a presently known polishing pad;

25 Figure 4(b) is a schematic representation of the structure of Figure 4(a) upon completion of a presently known polishing process, illustrating localized non-planarity;

Figure 5(a) is a schematic cross-section view of a non-cellular pad in accordance with a preferred embodiment of the present invention; and

30 Figure 5(b) is a schematic cross-section view of the structure of Figure 5(a) illustrating the enhanced planarity achievable with the substantially flat "lapping" pad of the present invention.

Detailed Description of Preferred Exemplary Embodiments

Referring now to Figure 1, presently known CMP processes typically employ a rigid foam polishing pad 10 to polish the surface of a workpiece 12, for example an integrated circuit layer. An abrasive slurry comprising a plurality of abrasive particles 14 in an aqueous medium is employed at the interface between the pad surface and workpiece surface.

With momentary reference to Figures 1 and 3, cellular pad 10 comprises a large number of randomly distributed open cells or bubbles, with exposed, irregularly shaped edges forming the junction between cells. Those edge surfaces 16 which come into contact with surface 18 of workpiece 12 are known as asperities, and support the load applied to pad 10 which results in frictional forces between pad 10 and workpiece 12 as pad 10 is moved laterally (e.g., in a circular planetary manner) with respect to workpiece 12 during the polishing process.

With continued reference to Figures 1 and 3, abrasive particles 14 within the slurry are urged onto surface 18 of workpiece 12 by asperities 16, creating high stress concentrations at the contact regions between asperities 16 and surface 18. Thus, Figure 1 illustrates some of the principle mechanical phenomena associated with known CMP processes.

Referring now to Figure 2, some of the principle chemical phenomena associated with known CMP techniques are illustrated. For example, in the case of polishing silica dialectrics, an ownwardly and impressed onto surface 18 of workpiece 12 by the pad, the chemical bonds which make up the structure of that layer of workpiece 12 in contact with pad 10 become mechanically stressed. The mechanical stress applied to these chemical bonds and their resultant strain increases the affinity of these bonds for hydroxide groups which are attached to abrasive particle 14. When the chemical bonds which comprise surface 18 of workpiece 12 are broken, silanols are liberated from surface 18 and carried away by the slurry. The liberation of these surface compounds facilitates the creation of a smooth, flat, highly planar surface 18.

In the context of a preferred embodiment of the present invention, a slurry is used to effect the chemical/mechanical polishing and planarization effects. More particularly, in the context of the present invention, a "slurry" suitably comprises a chemically and mechanically active solution, for example including abrasive particles coupled with chemically reactive agents. Suitable chemically reactive agents include hydroxides, but may also include highly basic or highly acidic ions: Suitable agents (e.g., hydroxides) are advantageously coupled to the abrasive particles within the slurry solution. In the context of a particularly preferred

embodiment, suitable abrasive particles within the slurry may be on the order of 10-200 nanometers in size in the source (dry) state, and most preferably about 30-80 nanometers. This is in contrast to traditional lapping solutions, which may include abrasives having sizes in the range of 0.5-100 micrometers. Suitable slurries in the context of the present invention may 5 also include oxidizing agents (e.g., potassium fluoride), for example in a concentration on the order of 5-20% by weight particle density, and most preferably about 11% by weight particle density.

Referring now to Figures 3 and 4(a), an exemplary workpiece 12 suitably comprises a silicon layer 22 having microelectronic structures 24 disposed thereon (or therein). 10 In accordance with the illustrated embodiment, microstructures 24 may comprise conductors, via holes, or the like, in the context of an integrated circuit. Workpiece 12 further comprises a dielectric layer 20 applied to the surface of silicon layer 22, which dielectric layer may function as an insulator between successive silicon layers in a multiple-layered integrated circuit.

During the semi-conductor manufacture process, dielectric 20 is placed over silicon layer 22 (and its associated electronic microstructures) in such a way that localized device topographies (e.g., ridges) 26 are formed in the dielectric layer corresponding to microstructures 24. It is these ridges, inter alia, which need to be eliminated during the CMP process to form an ideally uniform, flat, planar surface upon completion the CMP process. However, as is known in the art, present CMP techniques are not always capable of producing a sufficiently flat, planar surface, particularly for small device lithography, for example in the submicrometer (e.g., less than 2.5 micrometer) range.

Referring now to Figures 4(a) and 4(b), the asperities (e.g., projections) associated with the undersurface of polishing pad 10 contact dielectric surface 20 as surface 20 and pad 10 are moved relative to one another during the polishing process. A chemically and 25 mechanically active slurry or other suitable solution (not shown in Figure 4) is provided between the mating surfaces of workpiece 12 and pad 10 to facilitate the polishing process. As pad 10 moves relative to workpiece 12, the asperities associated with pad 10, in conjunction with the abrasive particles comprising the slurry, polish down device topographies (ridges) 26, 30 removing material from the ridges in accordance with the chemical and mechanical phenomena associated with the CMP process described above. In particular, the irregular edges which form the surfaces adjoining the cells of pad 10 tend to deflect or bend as they encounter

respective leading edges 28 of ridges 26, trapping abrasive particles between the asperities associated with pad 10 and the edges of respective device topographies 26, wearing down respective edges 28 at a faster rate than the device topography surfaces. During the course of the polishing process, ridges 26 are typically worn down until they are substantially co-planar with surface 18; however, it is known that this planarization process is incomplete. Hence, residual nodes or undulations 30 typically remain proximate microstructures 24 upon completion of the planarization process. Although surface 18(b) associated with workpiece 12 is certainly more highly planar upon completion of the CMP process than the surface 18(a) associated with workpiece 12 prior to completion of the planarization process, the existence of nodules can nonetheless be problematic, particularly in future generation integrated circuits wherein extremely high degrees of planarity are desired.

Referring now to Figure 5, a "lapping" pad 31 is suitably employed in a CMP process in lieu of polishing pad 10. In accordance with a particularly preferred embodiment, pad 31 suitably comprises a substantially flat surface in contact with workpiece 12, characterized by relatively few surface irregularities 34. In particular, surface irregularities 34 may comprise scratches or other non-planarities associated with the dressing of pad 31; alternatively, irregularities 34 may simply result from the welding together of polymers comprising pad 31, e.g., fused polyethylene, non-cellular urethanes, and the like.

In accordance with a further aspect of the present invention, pad 30 is suitably made from a porous material, which permits the adsorption and/or entrainment of suitable slurries, for example, aqueous high pH slurries comprising colloidal silica such as SC1 manufactured by the Cabot Corp. or Deltapol 4101 manufactured by SpeedFam Corporation of Chandler, Arizona, or cerium oxide slurred or low pH alumina slurries. In accordance with yet a further aspect of the present invention, pad 30 may suitably comprise any suitable flat material soft enough to resist damage to fragile integrated circuit device layers, e.g., flexibilized, epoxies. In this regard, it is desirable that pad 30 be desirably relatively pliable to permit the undersurface of pad 31 to conform to the global topography of a workpiece (e.g., wafers) without damaging the delicate microstructures 24 associated with workpiece 12 as pressures are applied between pad 31 and workpiece 12.

With continued reference to Figure 5, as pad 31 is moved laterally relative to workpiece 12, the downward force of pad 31 and, hence, the lateral shearing forces created at the interface between workpiece 12 and pad 31 are spread out over a substantially larger

surface area than was the case with pad 10. Consequently, substantially higher pressures may be applied between workpiece 12 and pad 31 than could be applied between workpiece 12 and pad 10 (see, Figure 4) without damaging the surface of workpiece 12 (e.g., microstructures 24). Moreover, the flat surface 32 of pad 31, as opposed to the asperities 16 associated with pad 10, 5 urge particles 14 onto surface 18 more uniformly, thereby resulting in a more uniform planar surface 18(b), as shown in Figure 5(b). Indeed, the use of a non-cellular or otherwise substantially flat surface associated with pad 31 greatly reduces the step height of the device microstructures associated with planarized surfaces 18(b).

Although the present invention is set forth herein in the context of the appended drawing figures, it should be appreciated that the invention to the specific forms shown. Various other modifications, variations, and enhancements in the design and arrangement of the non-cellular pad and various process parameters discussed herein may be made without departing from the spirit and scope of the present invention as set forth in the appended claims. For example, a preferred embodiment of the present invention is illustrated herein in the context of a dielectric layer over microelectronic structures; however, the present invention may be useful in the context of both multilevel integrated circuits and other small electronic devices, and for fine finishing, flattening and planarization of a broad variety of chemical, electro-mechanical, electromagnetic, resistive and inductive resistive devices, as well as for the fine finishing, flattening and planarization of optical and electro-optical and mechanical devices. These and other modifications may be made in the design and implementation of various aspects of the invention without departing from the spirit and scope of the invention as set forth in the appended claims.